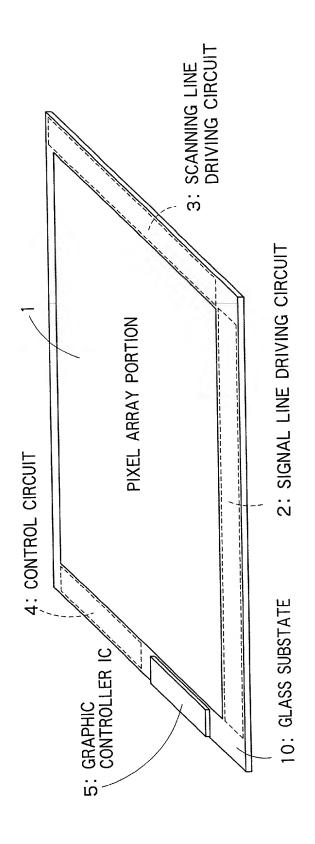
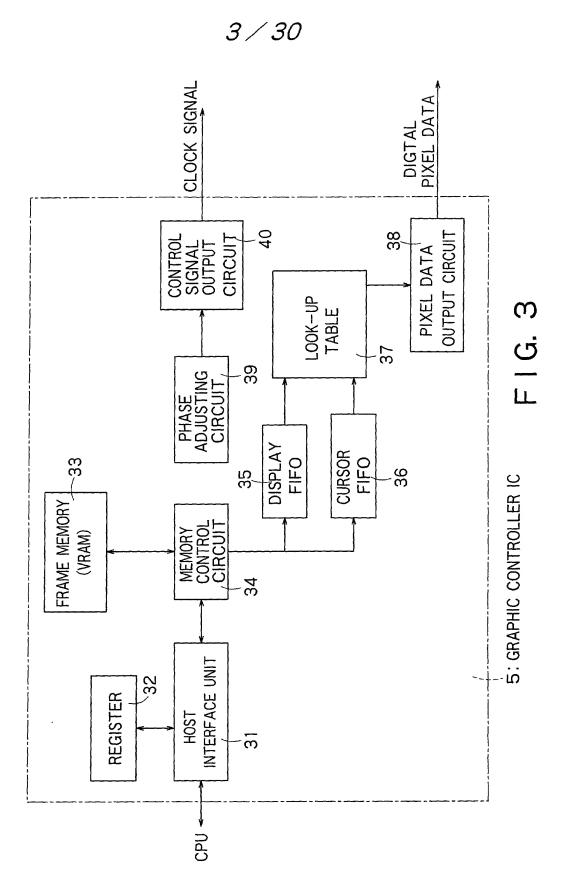


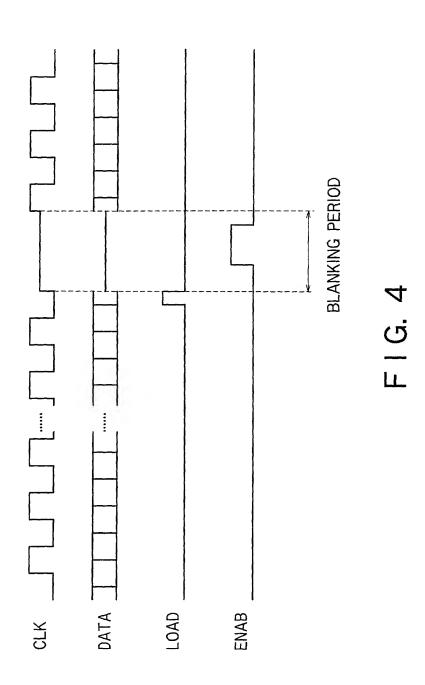
F I G. 1

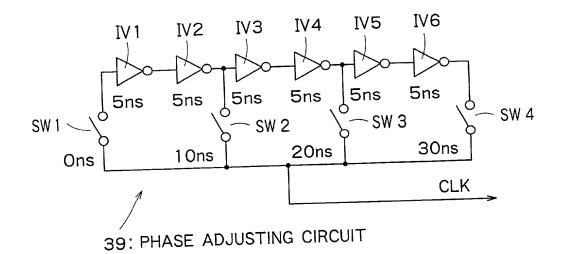


F1G. 2



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F I G. 5

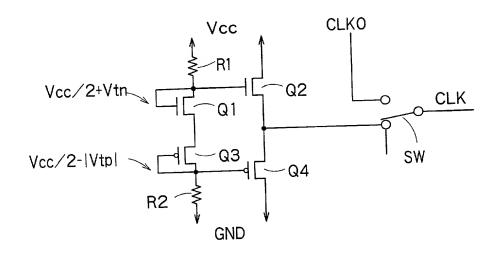
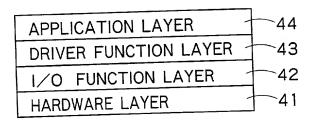
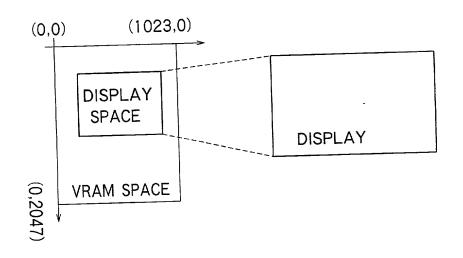


FIG. 6

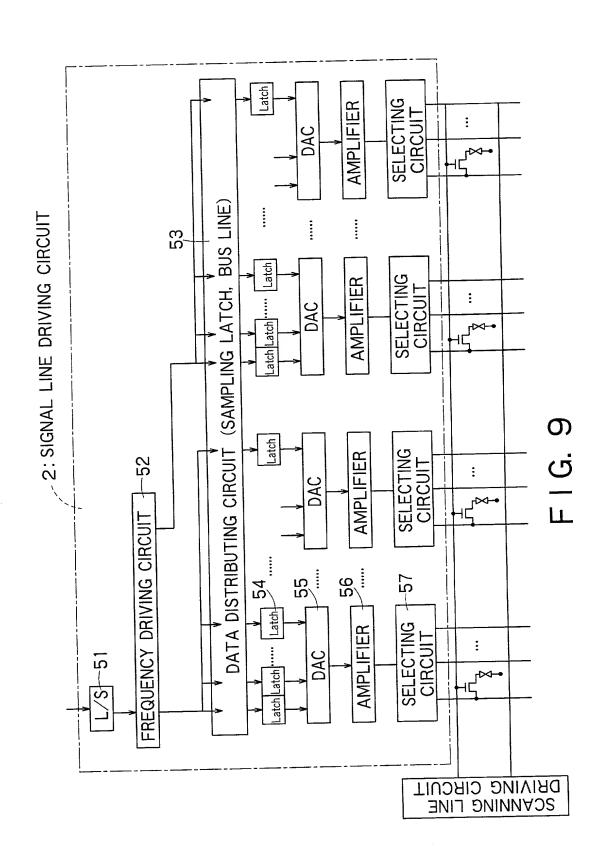




F I G. 7



F I G. 8





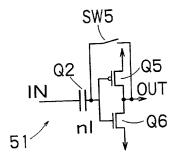


FIG. 10

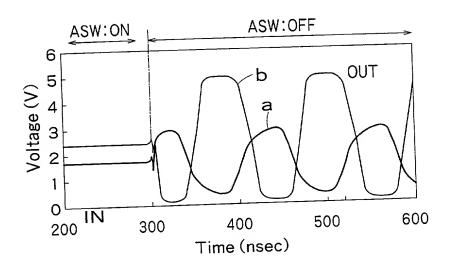


FIG. 11

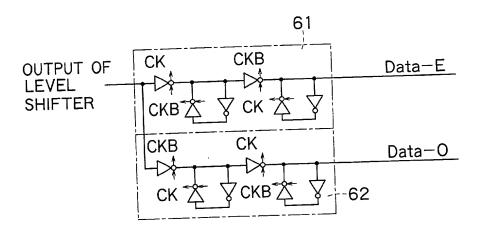
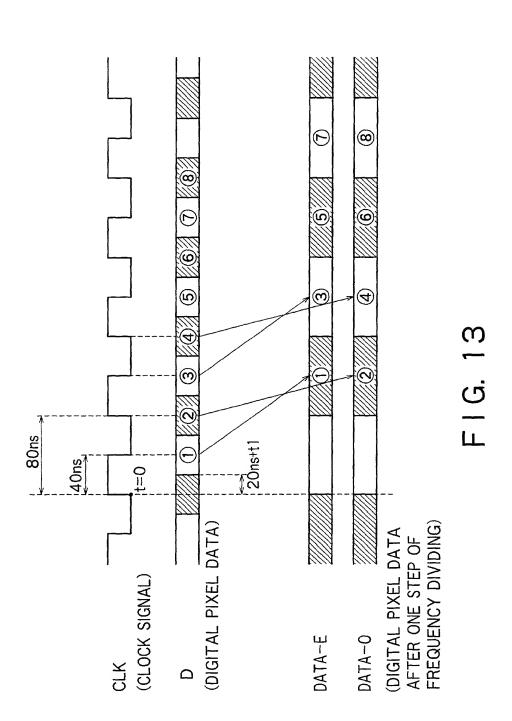


FIG. 12



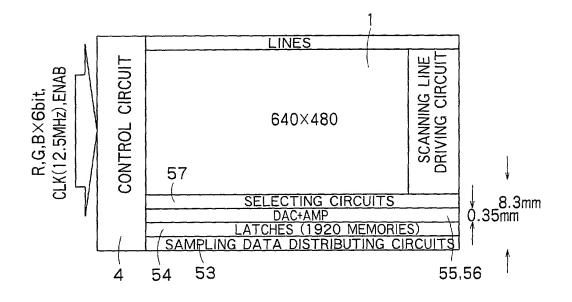


FIG. 14

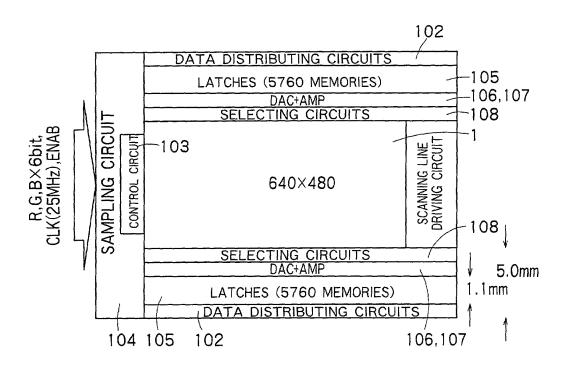
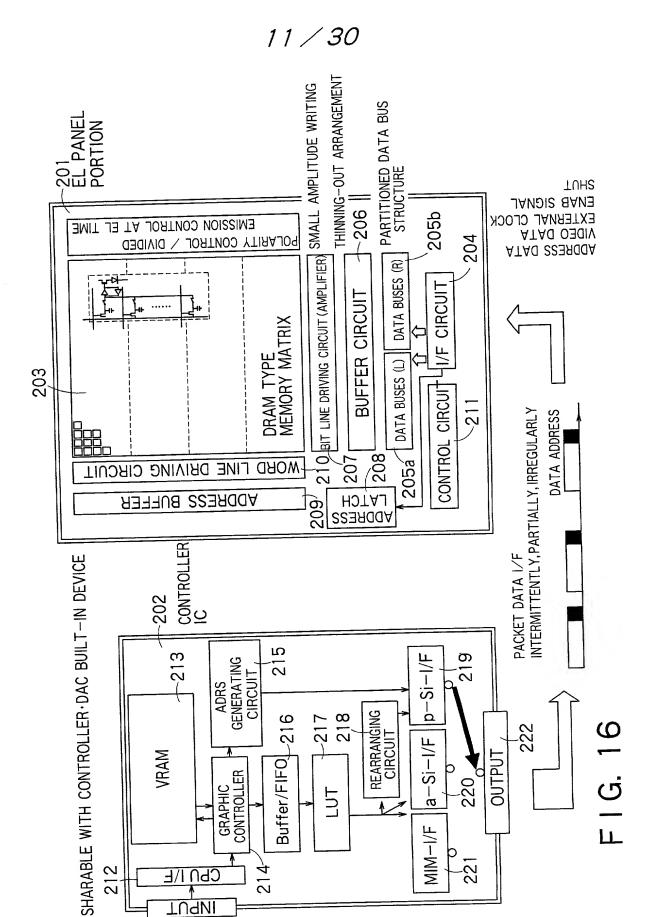
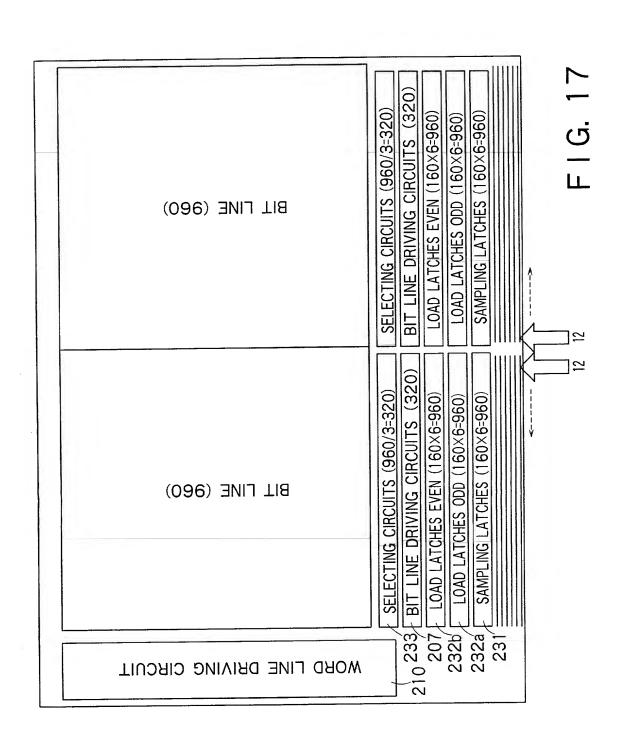


FIG. 15

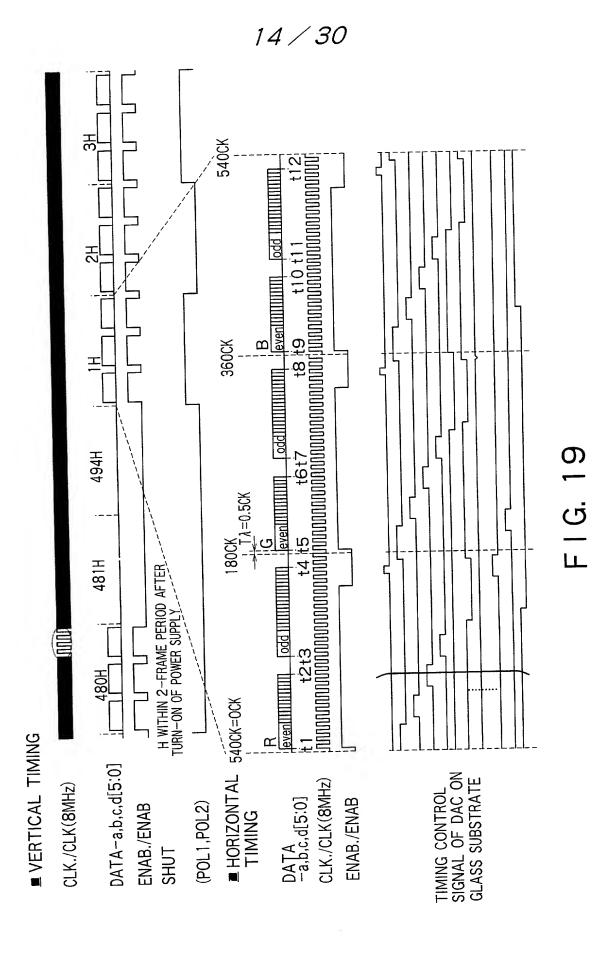
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... G306G310G314G318 .... G308G312G316G320 6 ... G334G330G328G322 8 ... G336G332G328G324 ... B306 B310 B314 B318 ... B308 B312 B316 B320 6 ... B334 B330 B326 B322 8 ... B336 B332 B328 B324 G640G636G632<del>G628\*\*\*</del> B10 B14 · B12 B16 · B12 B16 · B18630B626 · G2 G6 G10 G14 G4 G8 G12 G16 G638G634G630G626 ...R305R309R313R317BLK R2 R6 R10 R14 ...R307R311R315R319BLK R4 R8 R12 R16 ...R333R329R325R321BLK R638R634R630R626 ...R335R331R327R323BLK R640R636R632R628 B632B628 B634 B636 88 88 B305B309B313B317BLK B2 B307B311B315B319BLK B4 B333B329B325B321BLK B638F B335B331B327B323BLK B640F ... G305G309G313G317BLK G2 ... G307G311G315G319BLK G4 ... G333G329G325G321BLK G63 ... G335G331G327G323BLK G6 : : : DATA-a[5:0] R1 R5 R9 R13 DATA-b[5:0] R3 R7 R11 R15 DATA-d[5:0] R637 R633 R629 R625 DATA-d[5:0] R639 R635 R631 R627 6637 6633 6629 6625 B637 B633 B629 B625 B639 B635 B631 B627 G639 G635 G631 G627 813 153 <u>क</u> इ.इ.अ B11 B5/87 8 67 83 83 <u>B</u> 5 BLANKING PERIOD BLANKING PERIOD

F G. 18



SMALL AMPLITUDE	$\overline{\Box}$
WRITING DRIVER (BIT LINE DRIVING CIRCUIT)	
F I G. 20A	
	+
	怞
	+
<u></u>	
<u> </u>	
SMALL AMPLITUDE	

FIG. 20B

# 16/30 540CK DATA (FINAL LINE) DATA (FIRST LINE) Adrs H WITHIN 2-FRAME PERIOD AFTER TURN-ON OF POWER SUPPLY Adrs 540CK=0CK ■ VERTICAL TIMING DATA-a,b,c,d[5:0] ■ HORIZONTAL TIMING CLK./CLK(8MHz) CLK./CLK(8MHz) DATA \_a,b,c,d[5:0] EMAB./EMAB

ENAB SHUT

F1G. 21

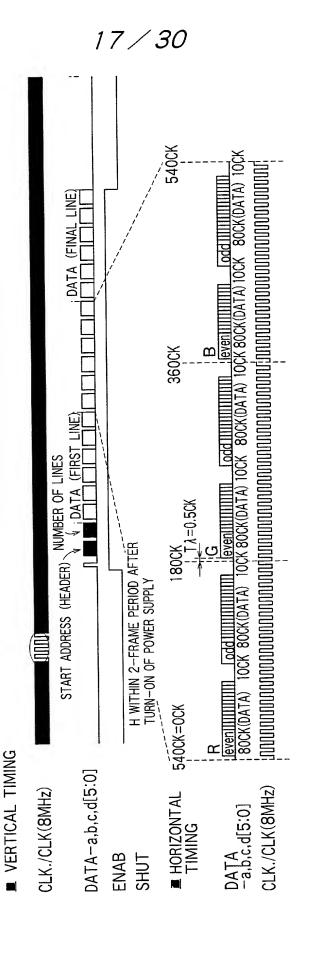
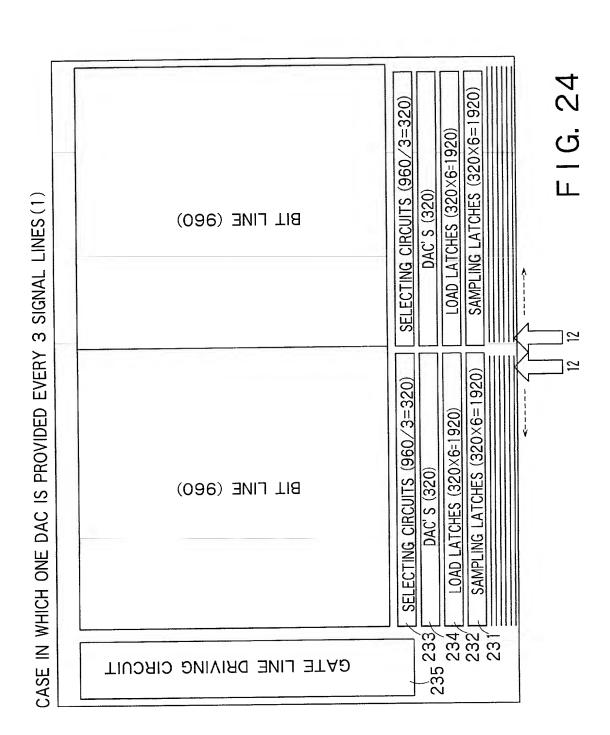


FIG. 22

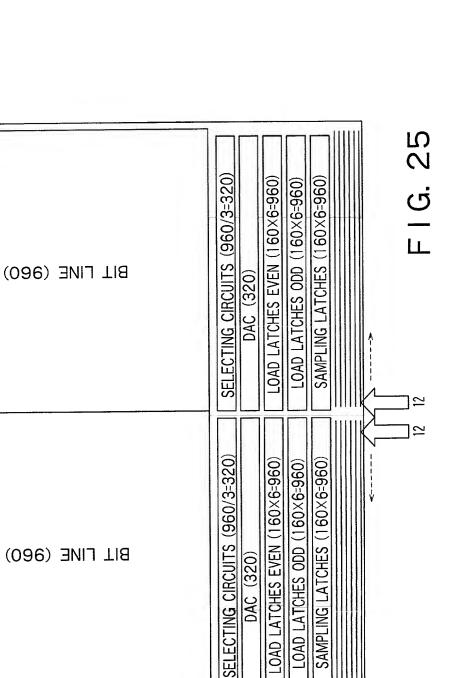
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OAD I

210 233 207 232b 232a 232a 231

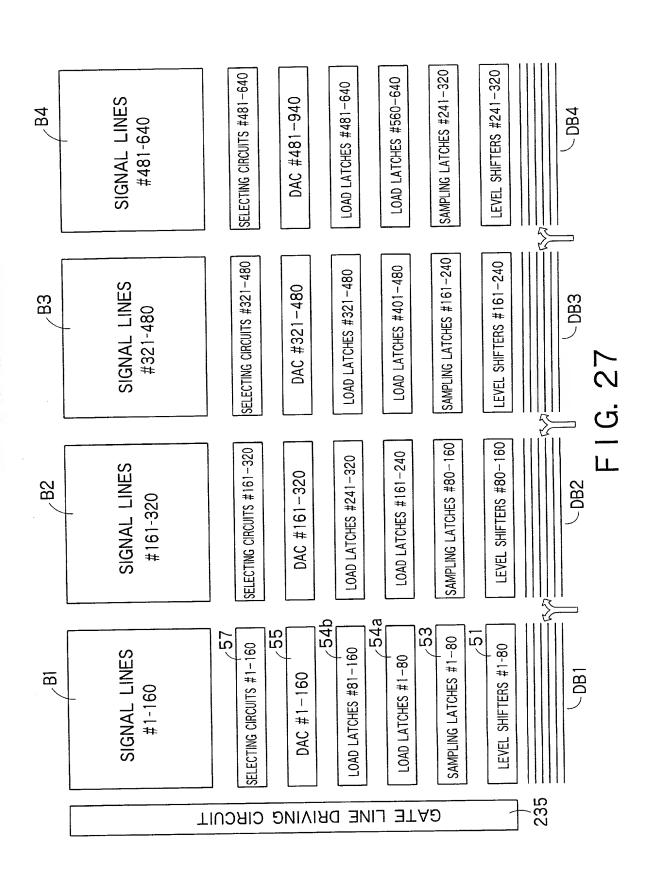
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GATE LINE DRIVING CIRCUIT

F1G. 26



The first state of the first sta

#### |R639 |R639 R639 R637 R637 S/L $S/\Gamma$ $S/\Gamma$ R479 R481 IR479 R479 R477 R477 $S/\Gamma$ $S/\Gamma$ S/LFIG. 28B FIG. 28C FIG. 28A |R321 R319 S/L $S/\Gamma$ S/LR163 R163 R161 R161 R159 | R161 SY **B**3 **R3** $\Xi$ $\Xi$ $\Xi$

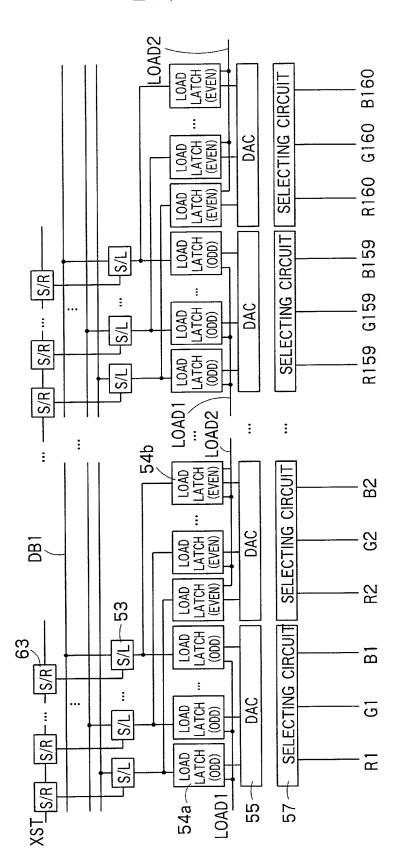


FIG. 29

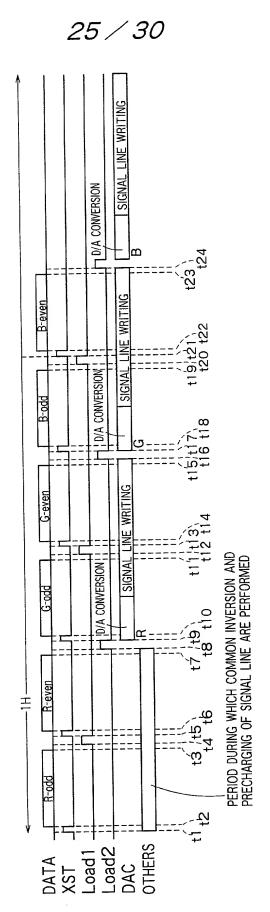
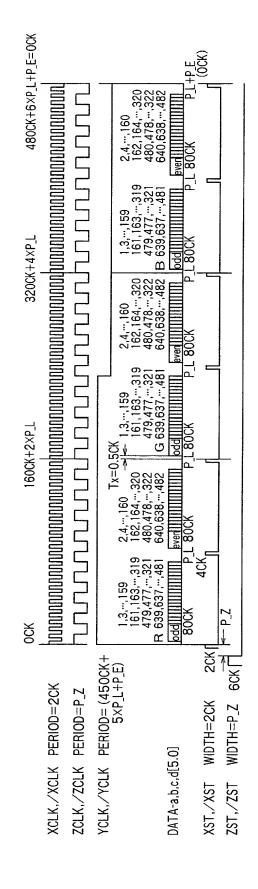


FIG. 30



五 G.3

DIGITAL PIXEL DATA
OPERATION MODE DESIGNATING SIGNAL

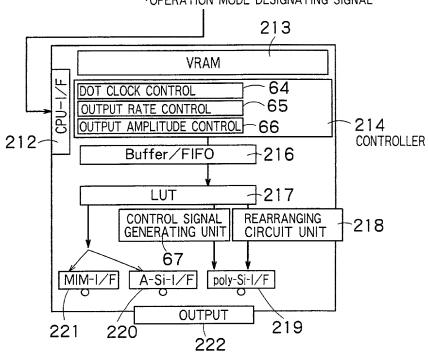


FIG. 32

·DIGITAL PIXEL DATA ·OPERATION MODE DESIGNATING SIGNAL

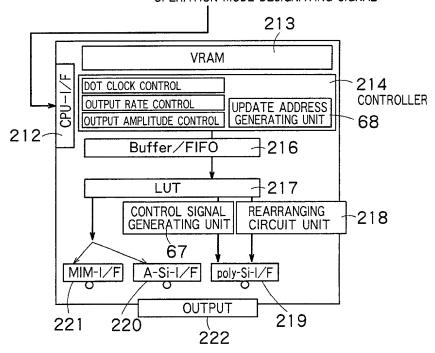


FIG. 33

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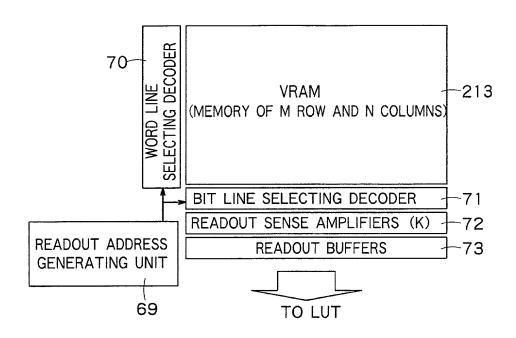


FIG. 34

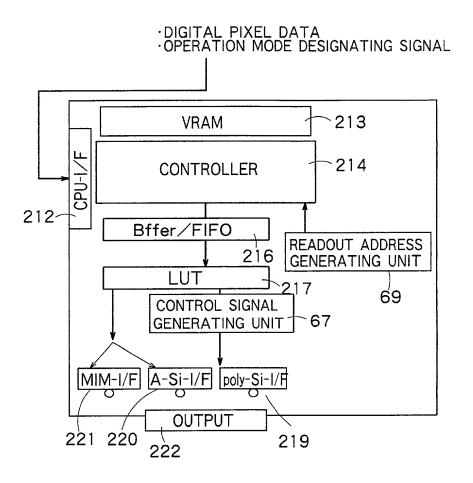


FIG. 35

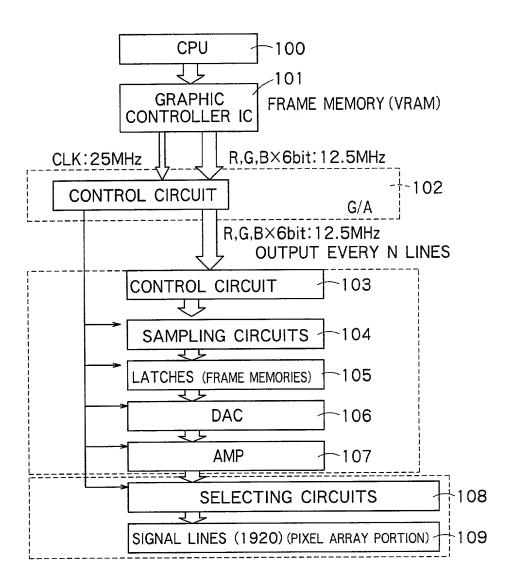


FIG. 36